



2816

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Shekhar Y. Borkar et al. Art Unit : 2816
Serial No.: 09/802,584 Examiner : Cox,
Filed: March 8, 2001
Title : A SYNCHRONOUS CLOCK GENERATOR FOR INTEGRATED CIRCUITS

Commissioner for Patents
Washington, D.C. 20231

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RESPONSE

This is in response to the action mailed October 3, 2001.
Reconsideration of the rejection is requested.

Claims 1-20 are pending. In the Action, the Examiner rejected claims 1-20 under 35 U.S.C. 102 (b) as being anticipated by Kawabata et al., U.S. Patent No. 5,936,912 ("Kawabata"). The Examiner also rejected claims 1-20 under 35 U.S.C. 102 (e) as being anticipated by Taniguchi et al., U.S. Patent No. 6,225,843 (Taniguchi). The Applicants respectfully traverse the rejections as follows.

Kawabata does not teach or suggest a delay circuit that is coupled to a delay lock loop circuit, which is responsive to a control signal from the delay lock loop circuit, to delay an input signal by a second period, as recited in claims 1, 9, and 14. Rather, Kawabata teaches a delay lock loop ("DLL") that includes a shift register, which controls the delay times of delay lines based on phase compare detection signals output by a phase comparator. [See e.g., Kawabata, Col.5:17-20.] Hence, the

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delay of the delay lines is set using multiple inputs to a phase comparator, which feeds a shift register. Depending on the contents of the shift register, the delay lines are subsequently set to a certain delay. However, there is no teaching or suggestion that one or more of the delay lines is responsive to a control signal from the other delay line. The Applicants teach that a control signal produced by a delay lock loop circuit may be used to set the delay of a delay circuit. This compares with a phase comparator with multiple inputs that sets a shift register as is taught by Kawabata. Thus, the delay lock loop circuit may be used as a reference to delay the delay circuit, and dependency on a duty cycle of an input signal may be eliminated.

Taniguchi, alone or in combination with Kawabata, does not teach or suggest a delay circuit that is coupled to a delay lock loop circuit, which is responsive to a control signal from the delay lock loop circuit to delay an input signal by a second period, as recited in claims 1, 9, and 14. Taniguchi teaches that a phase comparing section is used to generate a phase error signal, which is then fed to delay control circuits. [See e.g., Taniguchi, Col.1:39-46.] Taniguchi fails to disclose that one delay control circuit may be responsive to a control signal from another delay circuit. As explained above, the Applicants disclose that the delay circuit is responsive to a control signal from the delay lock loop circuit to delay the period on an input signal.

In view of the foregoing, the Applicants respectfully submit that claims 1, 9, and 14 are not anticipated by Kawabata or Taniguchi. Accordingly, the rejections to these claims should be withdrawn. Claims 2-8 are believed to be allowable